

DeSota
Serial no. 09/683,931
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Attorney docket no. BEA920010023

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In the claims:

1. (currently amended) A method comprising:
retrieving a cache entry for a desired memory address, the cache entry including data and a stored error-correcting code (ECC) based at least on the data and a memory address;
determining an ECC based on at least the data of the cache entry and the desired memory address; ~~and,~~
upon determining that the ECC based at least on the data of the cache entry and the desired memory address equals the stored ECC, concluding that the cache entry caches the desired memory address without error;
~~otherwise,~~
~~retrieving a second cache entry for the desired memory address, the cache entry including second data and a second stored ECC based at least on the second data and a second memory address;~~
~~determining a second ECC based at least on the second data of the second cache entry and the desired memory address; and,~~
~~upon determining that the second ECC based at least on the second data of the second cache entry and the desired memory address equals the second stored ECC, concluding that the second cache entry caches the desired memory address without error.~~
2. (original) The method of claim 1, further comprising, otherwise, retrieving a primary memory entry for the desired memory address.
3. (original) The method of claim 1, further comprising determining whether the cache entry caches the desired memory address with error.

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4. (original) The method of claim 1, further comprising determining whether the cache entry caches a memory address other than the desired memory address.
5. (cancelled)
6. (currently amended) The method of claim [[5]] 1, further comprising, otherwise, retrieving the desired memory address from primary memory.
7. (currently amended) The method of claim [[5]] 1, further comprising, otherwise, retrieving a third cache entry for the desired memory address, the cache entry including third data and a third stored ECC based on the third data and a third memory address; determining a third ECC based at least on the third data of the third cache entry and the desired memory address; and, upon determining that the third ECC based at least on the third data of the third cache entry and the desired memory address equals the third stored ECC, concluding that the third cache entry caches the desired memory address without error.
8. (original) The method of claim 1, wherein determining the ECC comprises determining the ECC based on the data of the cache entry and a tag of the desired memory address.
9. (original) The method of claim 1, wherein determining the ECC based on at least the data of the cache entry and the desired memory address comprises determining the ECC also based on a state of the cache as to the cache entry.
10. (currently amended) A system comprising:

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a primary memory having a number of memory entries corresponding to a plurality of memory addresses, each memory entry having data and a primary error-correcting code (ECC) based on the data;

a cache having a number of cache entries less than the number of memory entries, each cache entry having data and a stored ECC based at least on the data and a memory address to which the cache entry corresponds, the cache also storing a number of second cache entries less than the number of memory entries, each second cache entry having second data and a second stored ECC based at least on the second data and a second memory address to which the second cache entry corresponds; and,

a controller to retrieve desired memory addresses, the controller determining whether the cache entries for the desired memory addresses cache the desired memory addresses by determining ECCs based at least on the data of the cache entries and the desired memory addresses and comparing the ECCs determined to the stored ECCs of the cache entries,

wherein the controller, upon determining that the ECCs based on at least the data of the cache entries and the desired memory addresses equal the stored ECCs, concludes that the cache entries cache the desired memory addresses without error, and

wherein otherwise the controller retrieves second cache entries for the desired memory addresses, and determines second ECCs based at least on the second data of the second cache entries and the desired memory addresses.

11. (original) The system of claim 10, wherein the cache comprises a one-way cache, such that each memory entry of the primary memory can be cached in only one of the number of cache entries.

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12. (original) The system of claim 10, wherein the cache comprises a multi-way cache, such that each memory entry of the primary memory can be cached in more than one of the number of cache entries.

13. (original) The system of claim 10, wherein the controller, for each desired memory address, retrieves the memory entry for the desired memory address from the primary memory upon concluding that the ECC determined for the desired memory address does not equal the stored ECC for the cache entry for the desired memory address.

14. (original) The system of claim 10, wherein each of the stored ECC and the ECC determined is based on at least the data and a tag of the memory address.

15. (original) The system of claim 10, wherein each of the stored ECC and the ECC determined is also based on a cache state.

16. (original) The system of claim 10, wherein the system comprises a plurality of processors, such that the system is a multi-processor system.

17. (original) The system of claim 10, wherein the system comprises a single processor, such that the system is a single-processor system.

18.-20. (cancelled)